gate insulating layer comprises silicon dioxide.

46. (Amended) The semiconductor device of claim 80, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.

47. (Amended) The semiconductor device of claim 81, which is encapsulated.

60. (Twice Amended) The semiconductor device of claim 80, wherein said gate insulating layer comprises an oxide of silicon.

61. (Twice Amended) The semiconductor device of claim 81, wherein said gate insulating layer comprises silicon dioxide or silicon oxy nitride.

63. (Twice Amended) The semiconductor device of claim 80, wherein said gate insulating layer comprises silicon dioxide.

65. (Amended) The semiconductor device of claim 80, comprising deuterium atoms from said post-fabrication passivation covalently bonded at said interface.

69 (Twice Amended) The device as recited in claim 81, wherein said transistor gate is comprised of polycrystalline silicon.

72. (Twice Amended) The device as recited in claim 81 wherein said substrate is